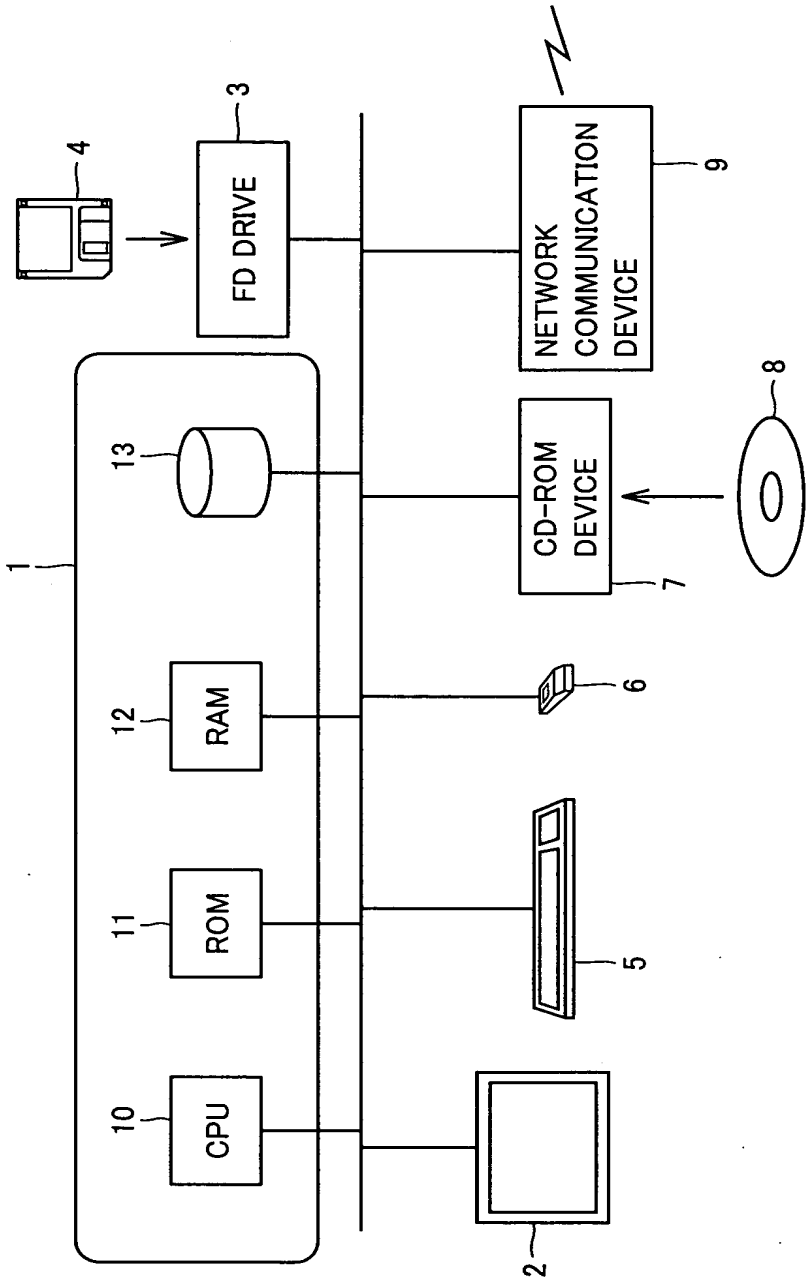

FD DRIVE
NETWORK COMMUNICATION DEVICE
CD-ROM DEVICE
RAM
ROM
CPU
1
2
3
4
5
6
7
8
9
10
11
12
13

FIG.1

FIG.2

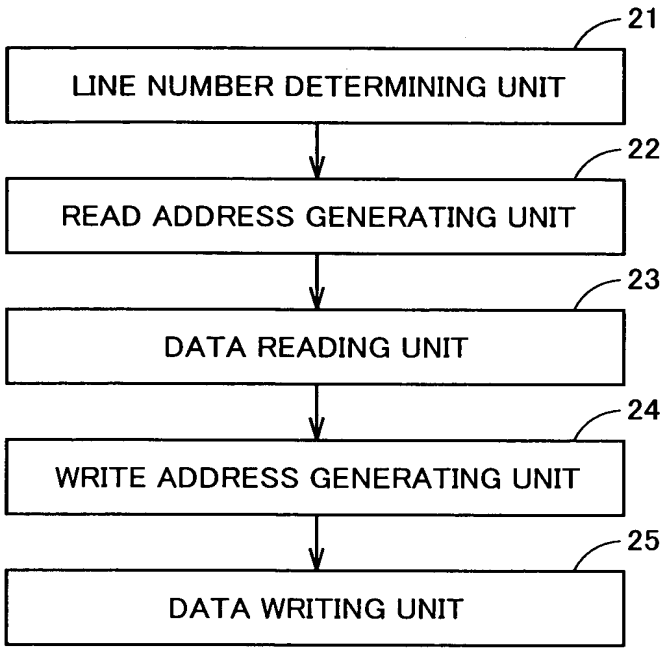

21
LINE NUMBER DETERMINING UNIT
22
READ ADDRESS GENERATING UNIT
23
DATA READING UNIT
24
WRITE ADDRESS GENERATING UNIT
25
DATA WRITING UNIT

FIG.3

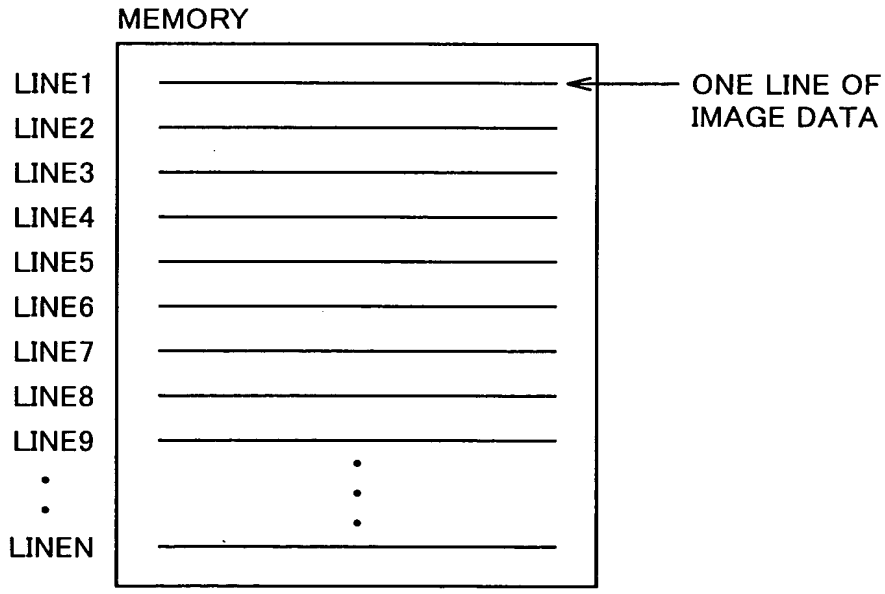

MEMORY
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE9
LINEN
ONE LINE OF IMAGE DATA

FIG.4A

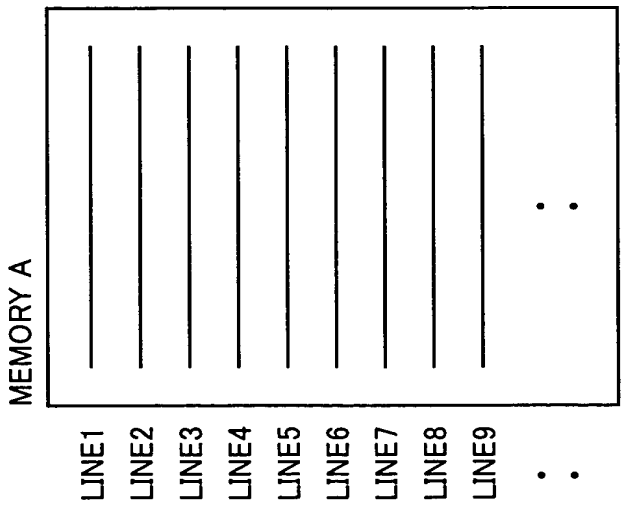
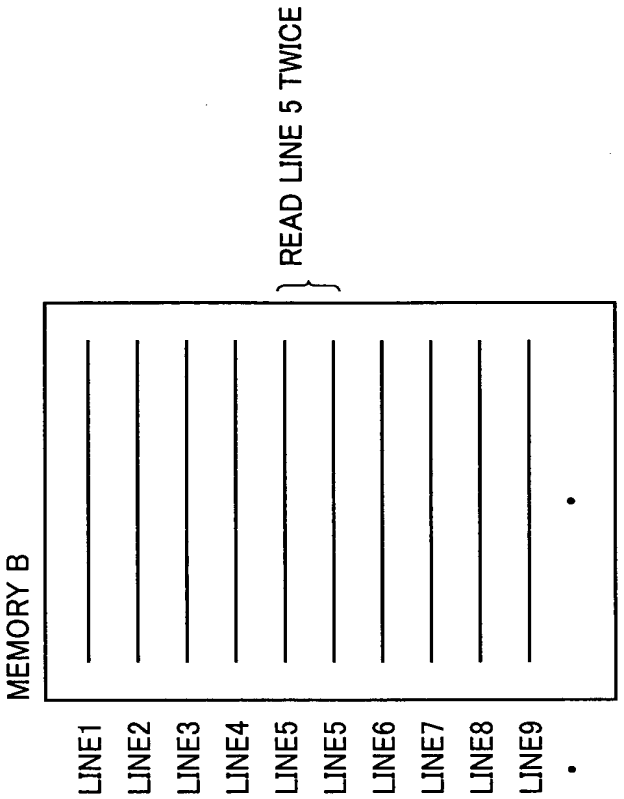

MEMORY A
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE9
DATA READ

FIG.4B


READ LINE 5 TWICE
MEMORY B
LINE1
LINE2
LINE3
LINE4
LINE5
LINE5
LINE6
LINE7
LINE8
LINE9

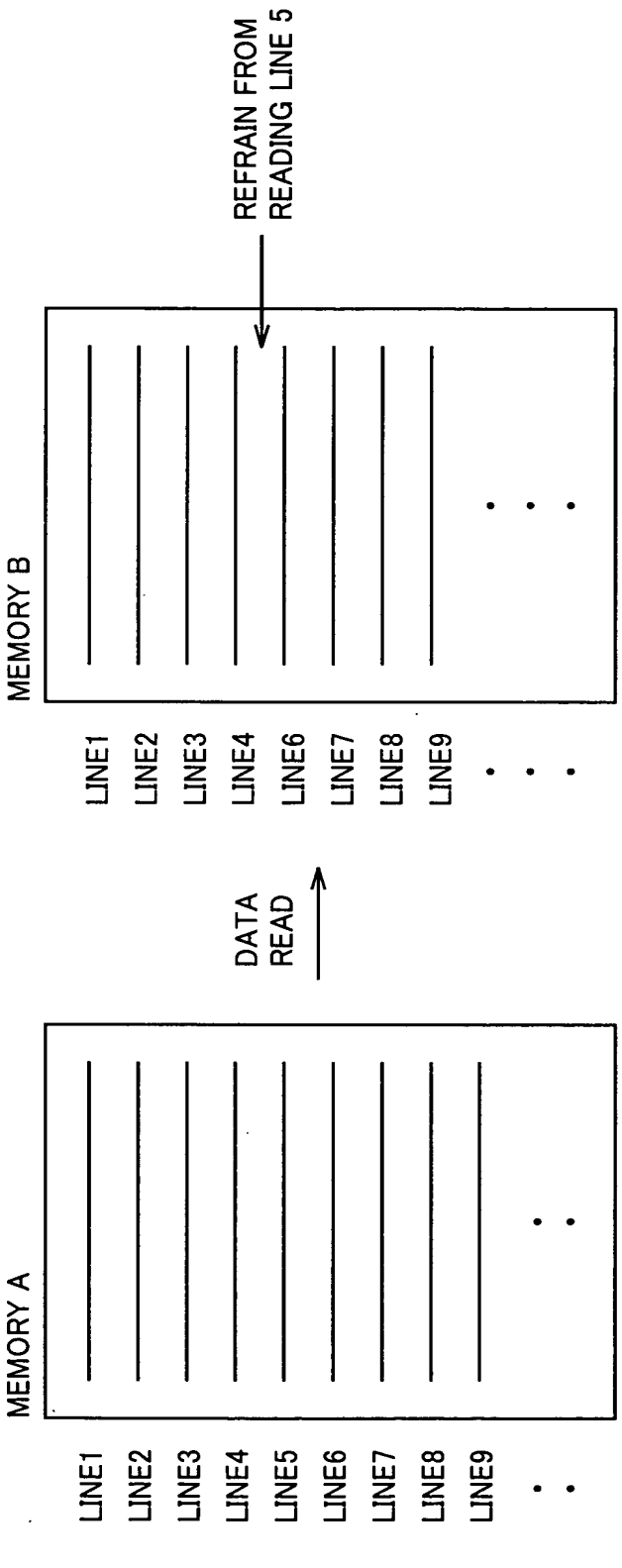
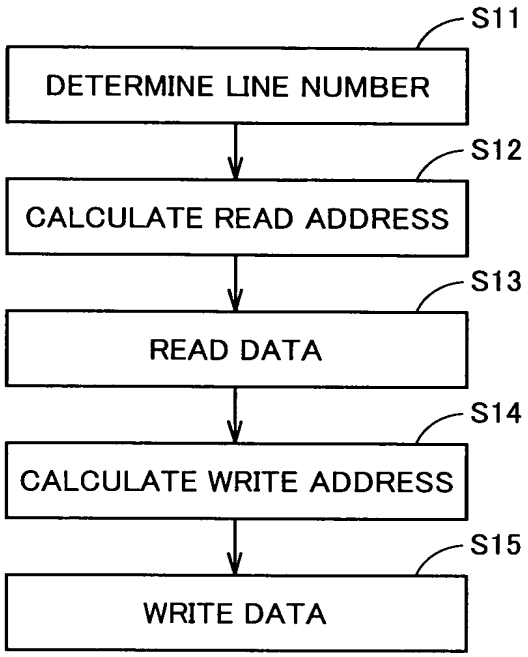

REFRAIN FROM READING LINE 5
MEMORY B
LINE1
LINE2
LINE3
LINE4
LINE6
LINE7
LINE8
LINE9
DATA READ
MEMORY A
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE9

FIG.5B

FIG.5A

FIG.6


S11
DETERMINE LINE NUMBER
S12
CALCULATE READ ADDRESS
S13
READ DATA
S14
CALCULATE WRITE ADDRESS
S15
WRITE DATA

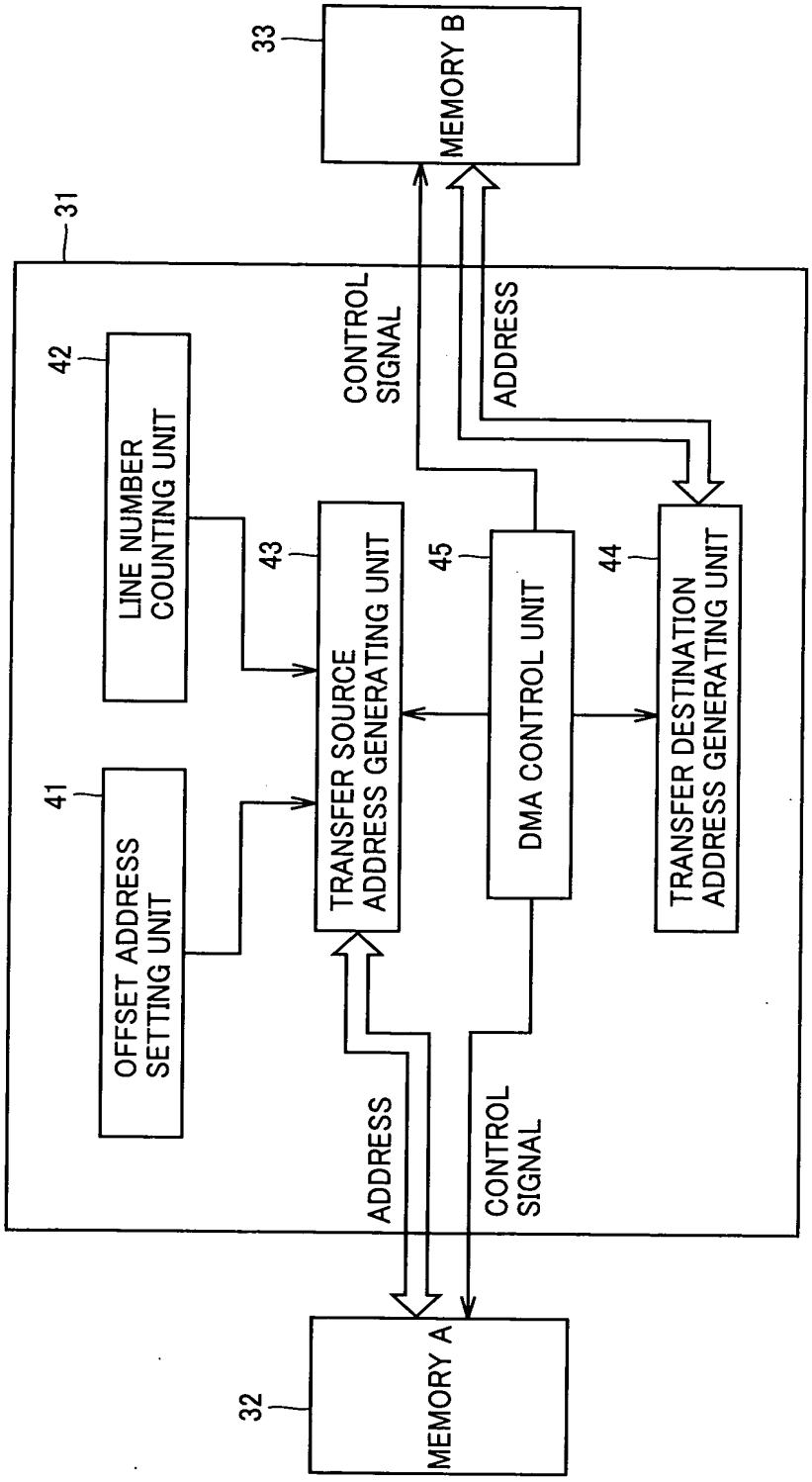

33
MEMORY B
31
CONTROL SIGNAL
ADDRESS
42
LINE NUMBER COUNTING UNIT
43
TRANSFER SOURCE ADDRESS GENERATING UNIT
45
DMA CONTROL UNIT
44
TRANSFER DESTINATION ADDRESS GENERATING UNIT
41
OFFSET ADDRESS SETTING UNIT
ADDRESS
CONTROL SIGNAL
32
MEMORY A

FIG.7

FIG.8A

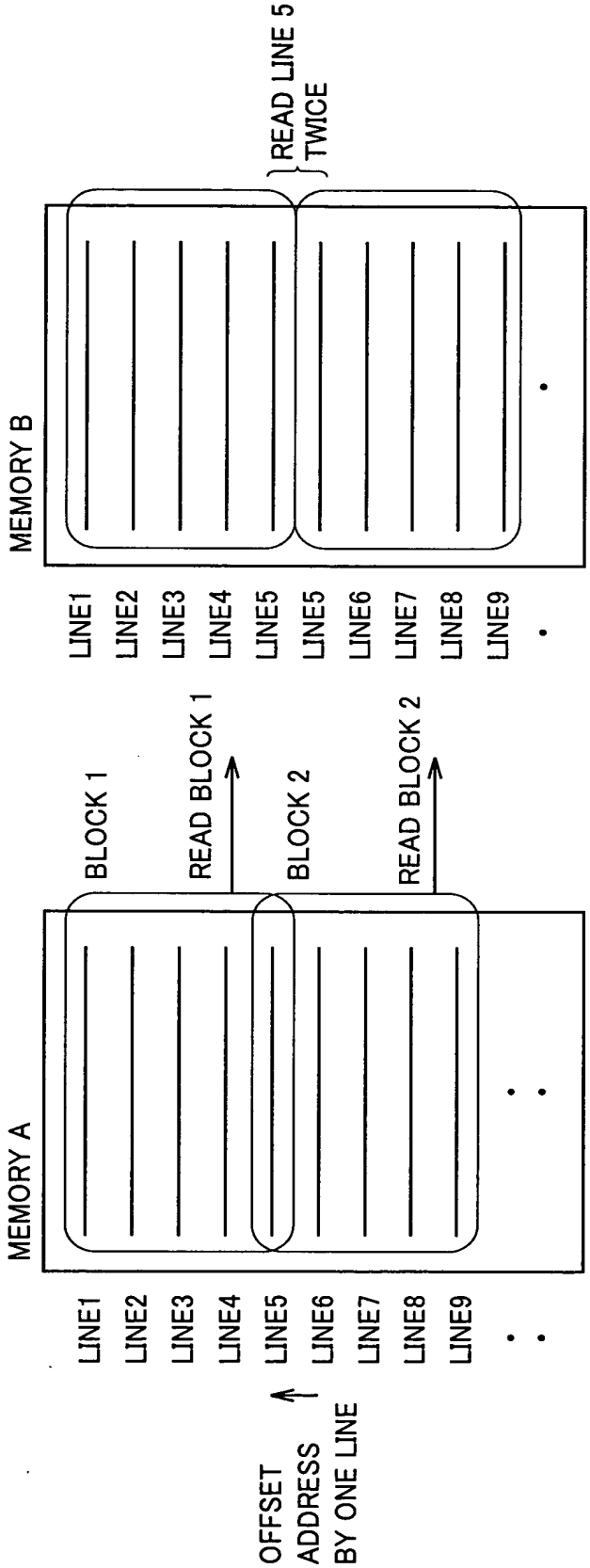

MEMORY A
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE9
BLOCK 1
READ BLOCK 1
BLOCK 2
READ BLOCK 2
OFFSET ADDRESS BY ONE LINE

FIG.8B


MEMORY B
LINE1
LINE2
LINE3
LINE4
LINE5
LINE5
LINE6
LINE7
LINE8
LINE9
READ LINE 5 TWICE

FIG.9A

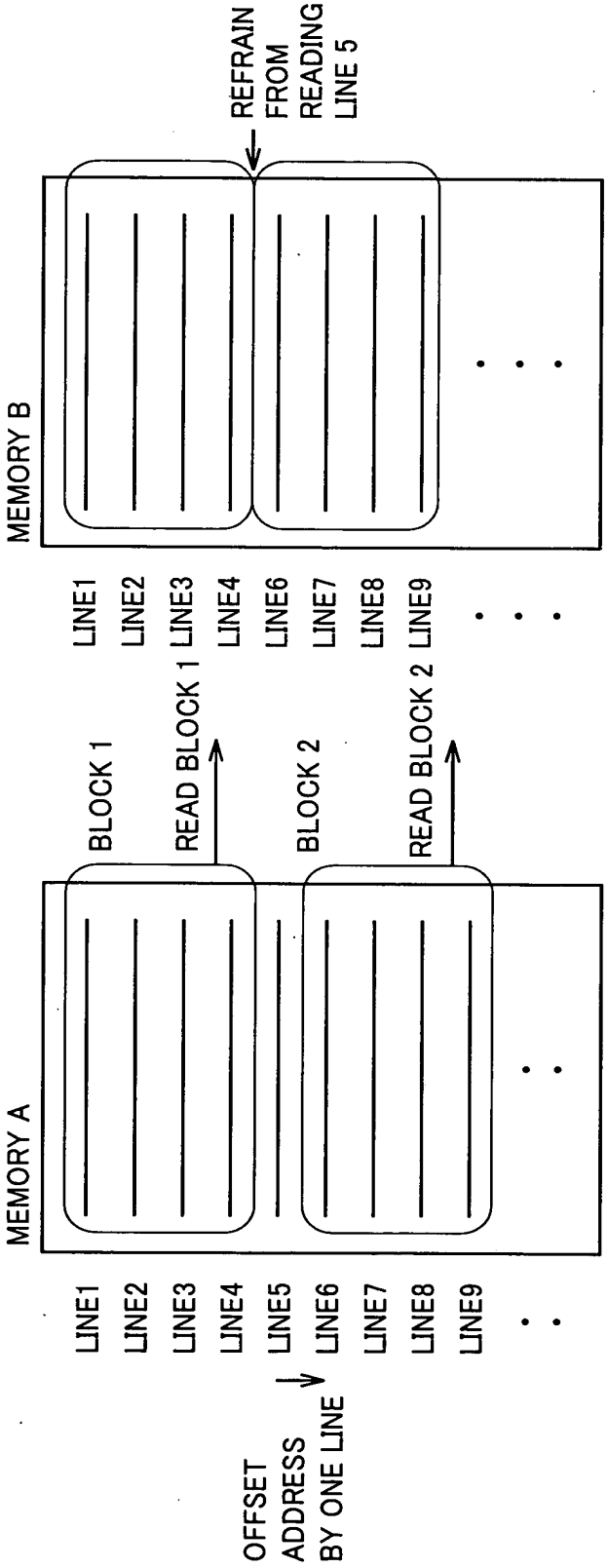

MEMORY A
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE9
BLOCK 1
READ BLOCK 1
BLOCK 2
READ BLOCK 2
OFFSET ADDRESS BY ONE LINE

FIG.9B


MEMORY B
LINE1
LINE2
LINE3
LINE4
LINE6
LINE7
LINE8
LINE9
REFRAIN FROM READING LINE 5